Abstract of the Disclosure:

A packet receiving circuit 11 splits the packet received from a transmission channel 1 into a fixed length of cells and outputs the cells, a search key extracting circuit 12 extracts a predetermined search key from the above-mentioned cells, a CAM 13 performs retrieval based on the above-mentioned search key and outputs a memory address corresponding to the search key, a matching entry address receiving and associative data address transmitting circuit 14 calculates the memory address of an associative data memory 15 based on the above-mentioned memory address and outputs the information stored in the associative data memory 15 as associative data, a search result (associative data) receiving circuit 16 receives the above-mentioned associative data and performs header-updating and destination address of the above-mentioned cells, and a packet transmitting circuit 17 outputs the above-mentioned cells in the form of a packet to a transmission channel 2.